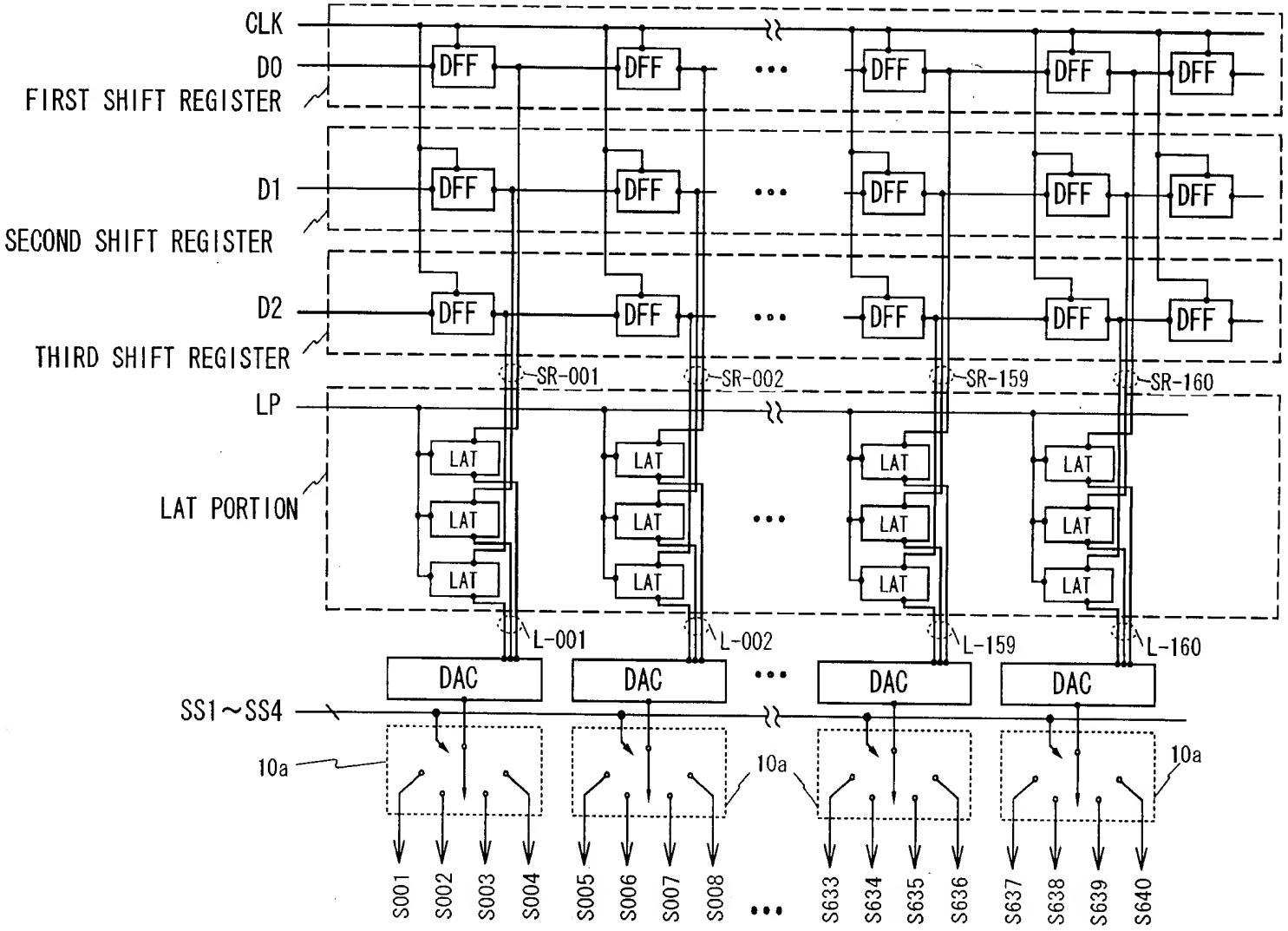

CLK
D0
FIRST SHIFT REGISTER
D1
SECOND SHIFT REGISTER
D2
THIRD SHIFT REGISTER
LP
LAT PORTION
SS1~SS4
10a
DFF
LAT
SR-001
SR-002
SR-159
SR-160
L-001
L-002
L-159
L-160
DAC
S001
S002
S003
S004
S005
S006
S007
S008
S633
S634
S635
S636
S637
S638
S639
S640
TO SIGNAL LINES

FIG. 1

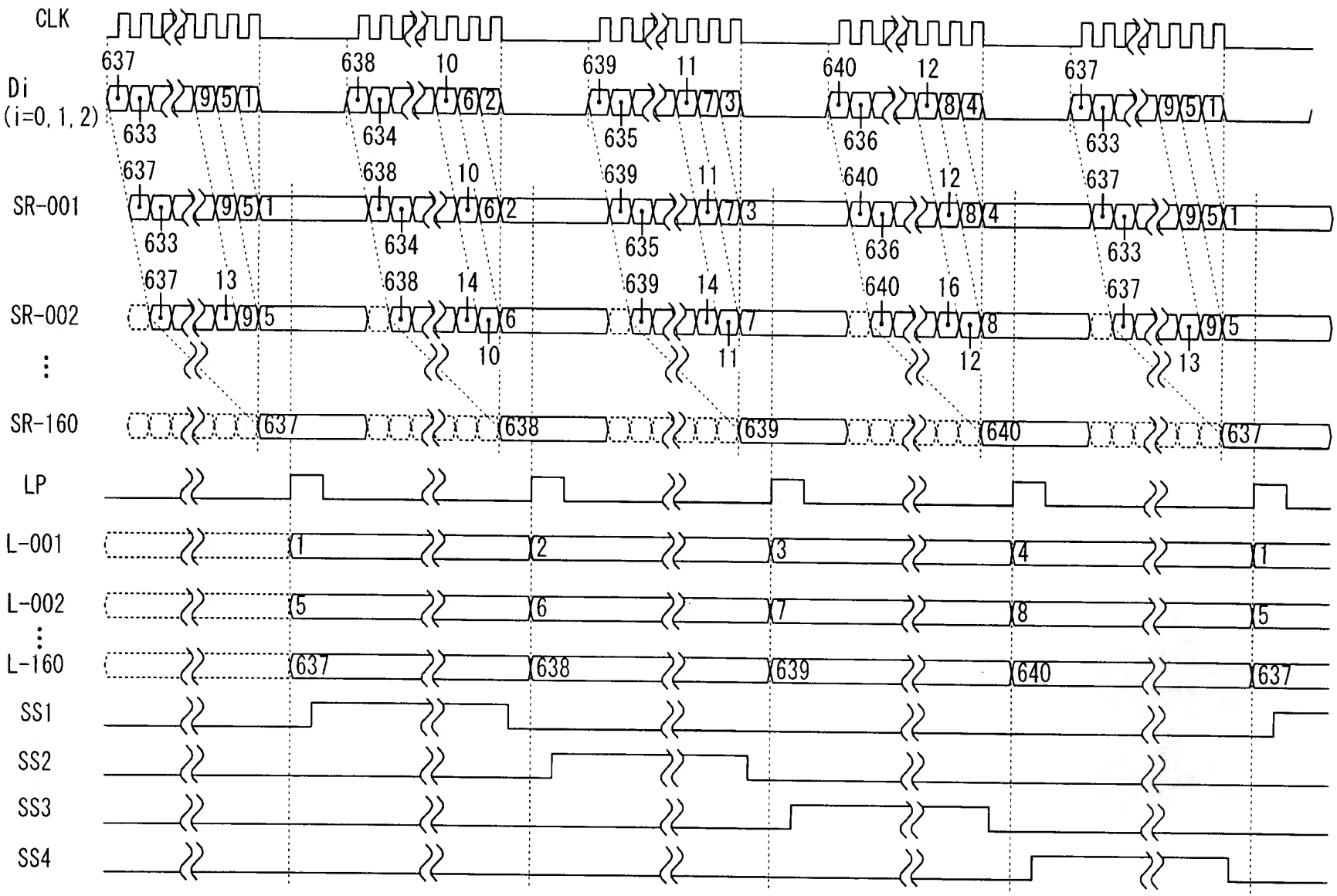

CLK
Di
(i=0, 1, 2)
SR-001
SR-002
SR-160
LP
L-001
L-002
L-160
SS1
SS2
SS3
SS4

FIG. 2

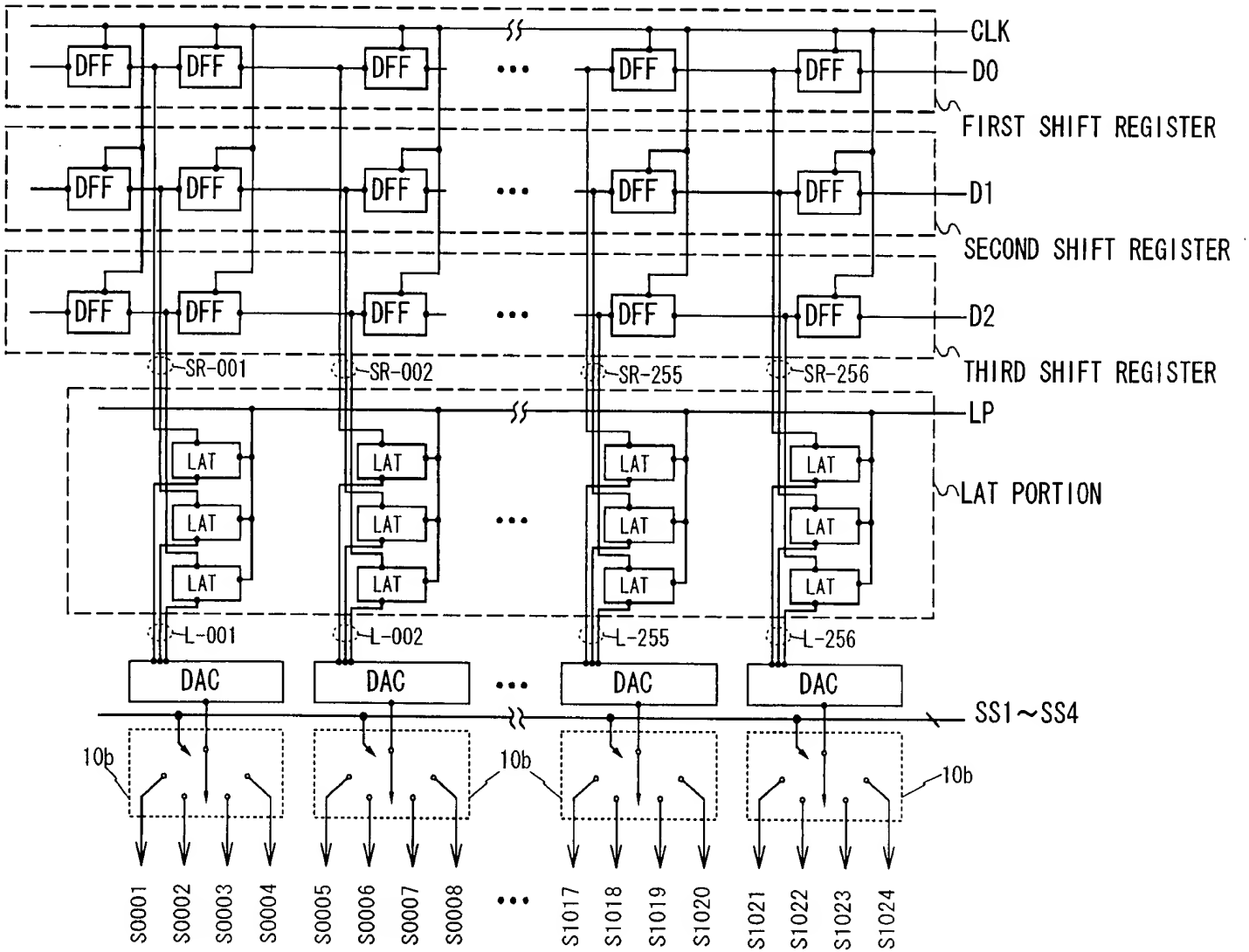

CLK
DO
FIRST SHIFT REGISTER
D1
SECOND SHIFT REGISTER
D2
THIRD SHIFT REGISTER
LP
LAT PORTION
SS1~SS4
DFF
LAT
DAC
SR-001
SR-002
SR-255
SR-256
L-001
L-002
L-255
L-256
10b
S0001
S0002
S0003
S0004
S0005
S0006
S0007
S0008
S1017
S1018
S1019
S1020
S1021
S1022
S1023
S1024
TO SIGNAL LINES

FIG. 3

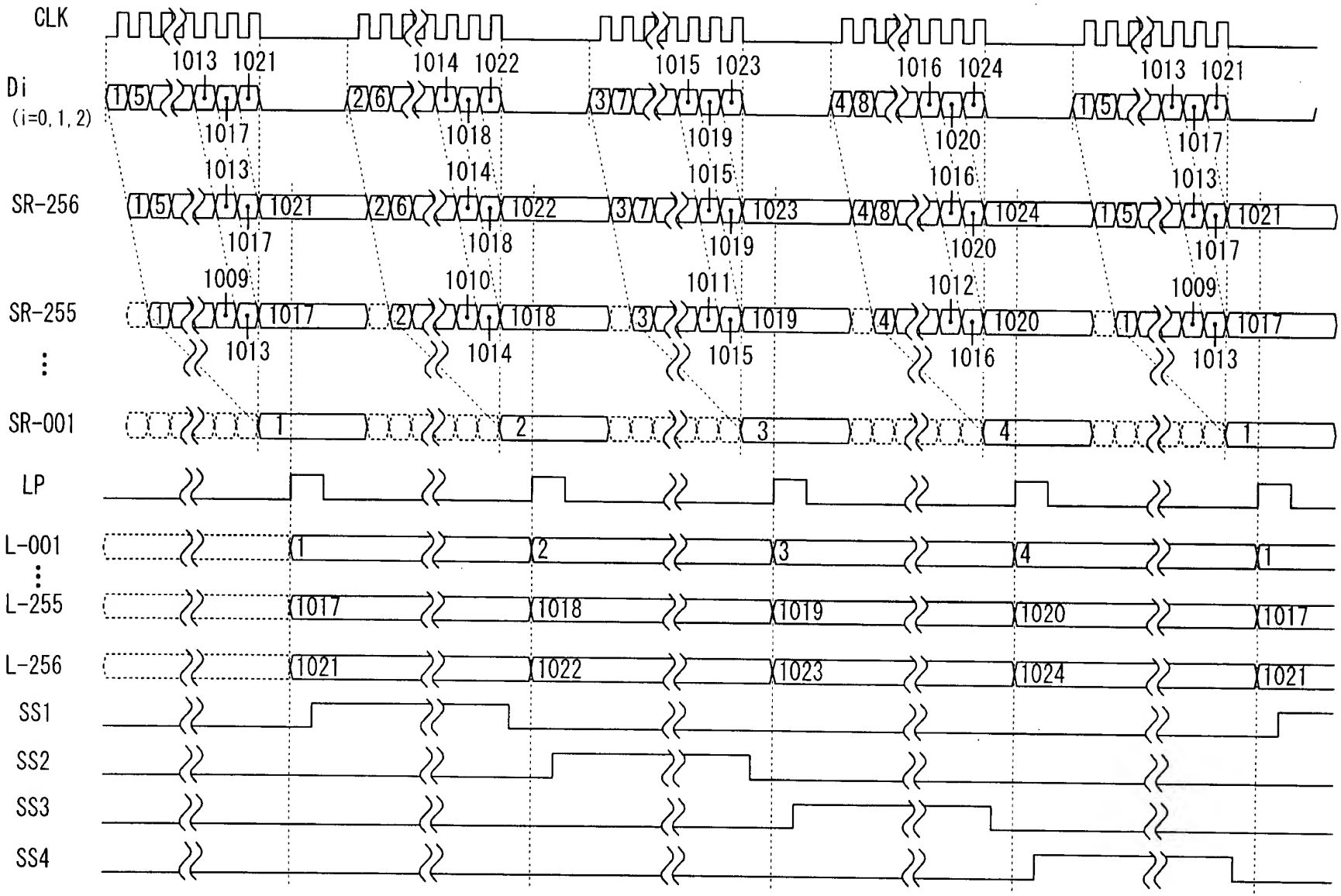

CLK
Di
(i=0, 1, 2)
SR-256
SR-255
SR-001
LP
L-001
L-255
L-256
SS1
SS2
SS3
SS4
1013 1021
1014 1022
1015 1023
1016 1024
1013 1021
1017
1018
1019
1020
1017
1013
1014
1015
1016
1013
1009
1010
1011
1012
1009
1021
1022
1023
1024
1021
1017
1018
1019
1020
1017
1013
1014
1015
1016
1013
1
2
3
4
1
1017
1018
1019
1020
1017
1021
1022
1023
1024
1021

FIG. 4

FIG. 5A

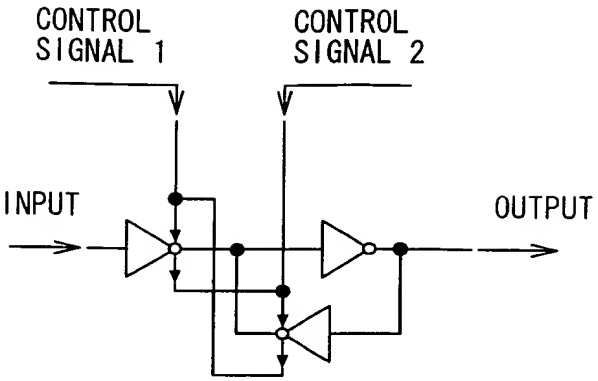


FIG. 5B

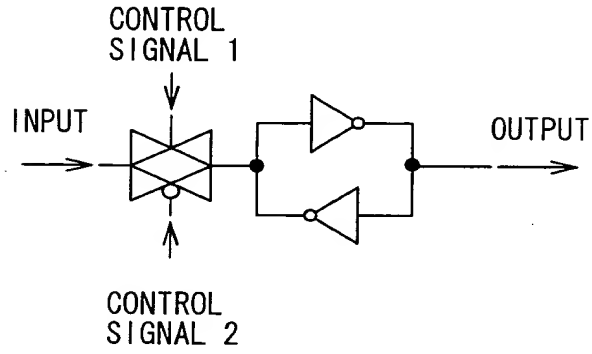
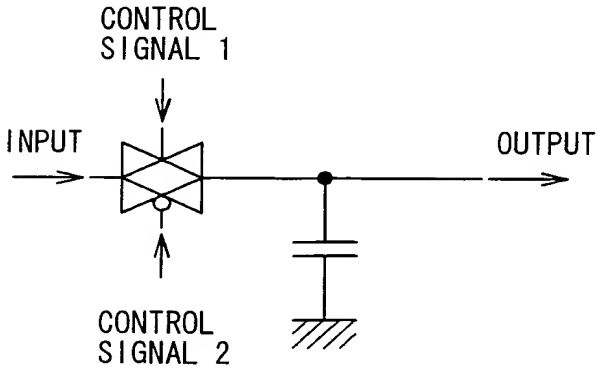


FIG. 5C



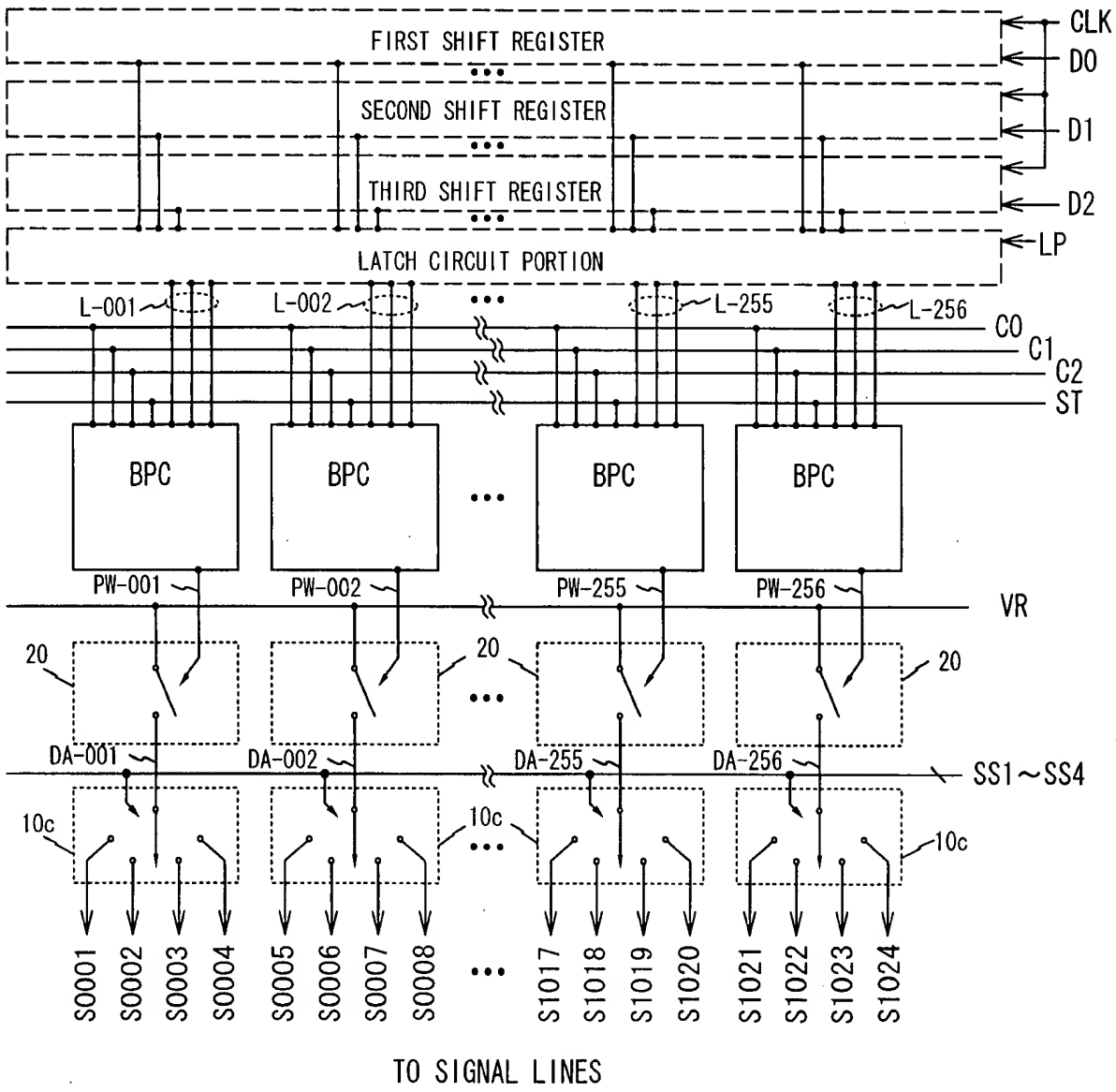

FIRST SHIFT REGISTER
SECOND SHIFT REGISTER
THIRD SHIFT REGISTER
LATCH CIRCUIT PORTION
CLK
DO
D1
D2
LP
L-001
L-002
L-255
L-256
CO
C1
C2
ST
BPC
PW-001
PW-002
PW-255
PW-256
VR
20
DA-001
DA-002
DA-255
DA-256
SS1~SS4
10c
S0001
S0002
S0003
S0004
S0005
S0006
S0007
S0008
S1017
S1018
S1019
S1020
S1021
S1022
S1023
S1024
TO SIGNAL LINES

FIG. 6

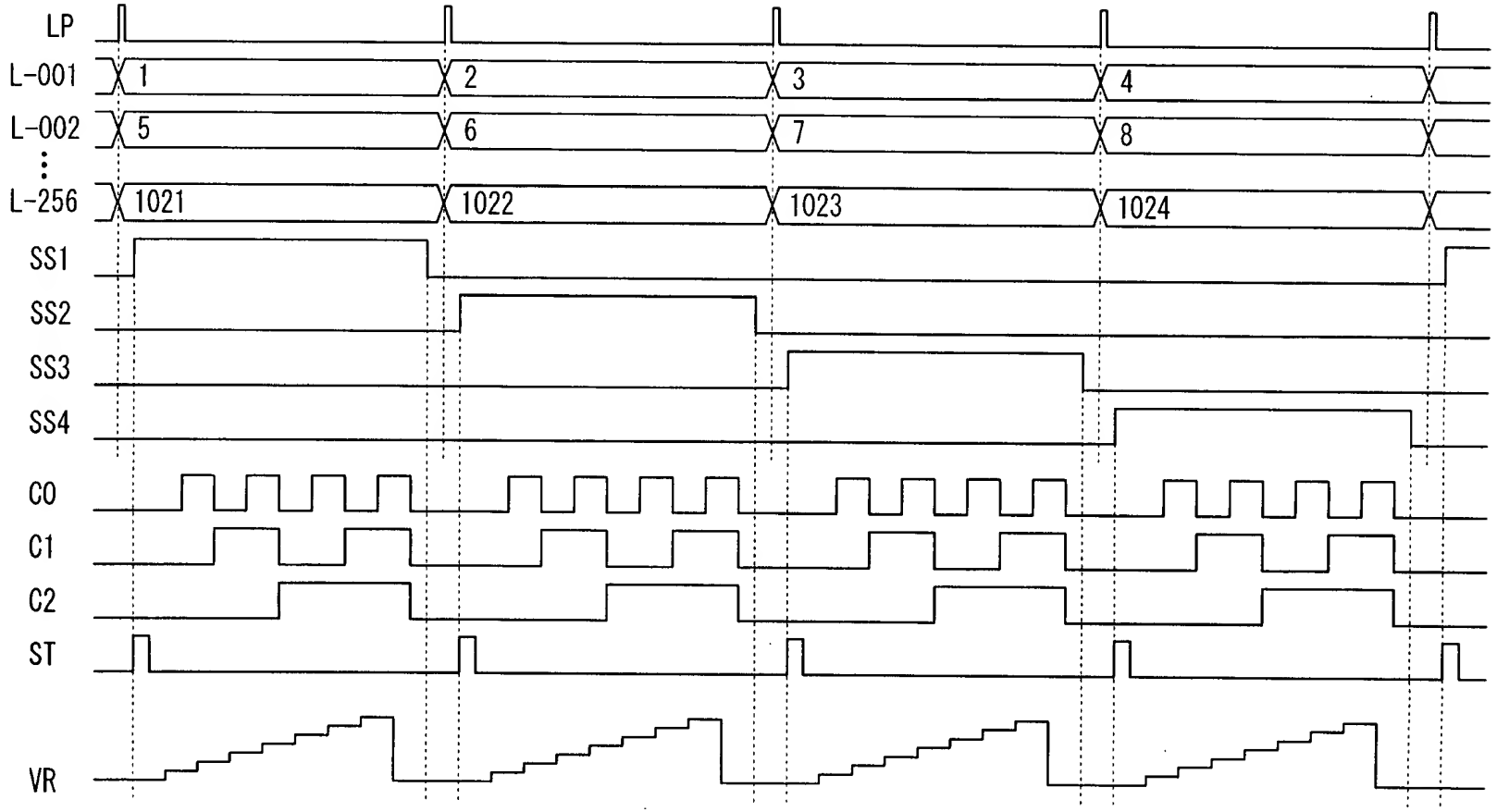

LP
L-001
L-002
L-256
1
2
3
4
5
6
7
8
1021
1022
1023
1024
SS1
SS2
SS3
SS4
C0
C1
C2
ST
VR

FIG. 7

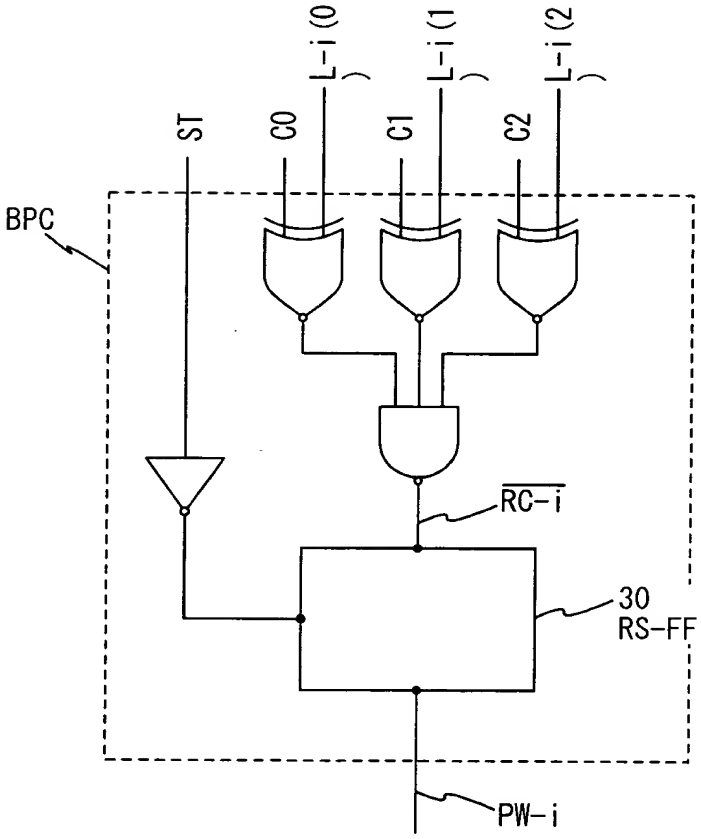


FIG. 8

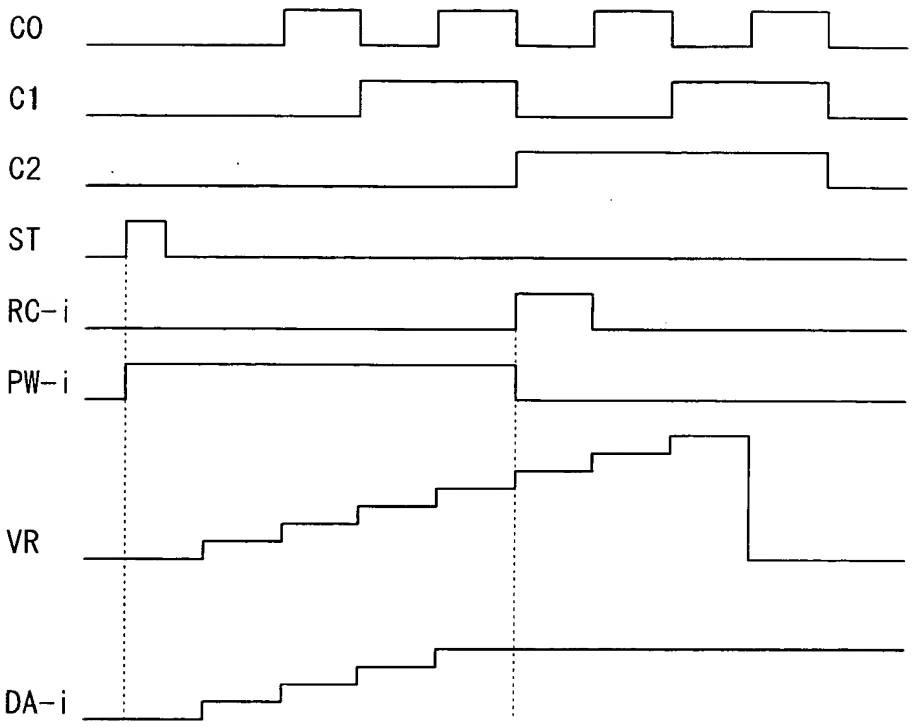


FIG. 9

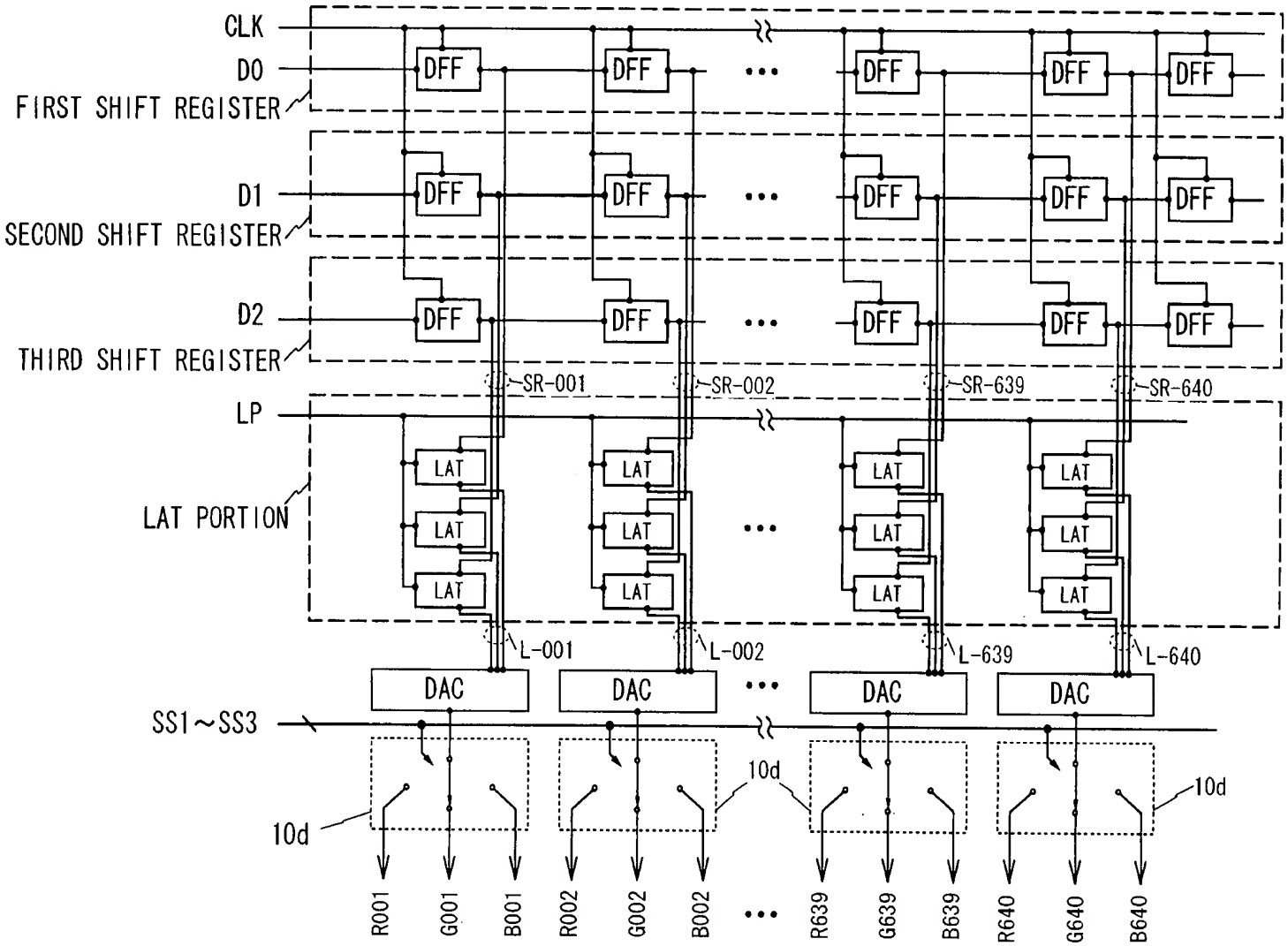

CLK
D0
FIRST SHIFT REGISTER
D1
SECOND SHIFT REGISTER
D2
THIRD SHIFT REGISTER
LP
LAT PORTION
SS1~SS3
DFF
LAT
DAC
SR-001
SR-002
SR-639
SR-640
L-001
L-002
L-639
L-640
10d
R001
G001
B001
R002
G002
B002
R639
G639
B639
R640
G640
B640
TO SIGNAL LINES

FIG. 10

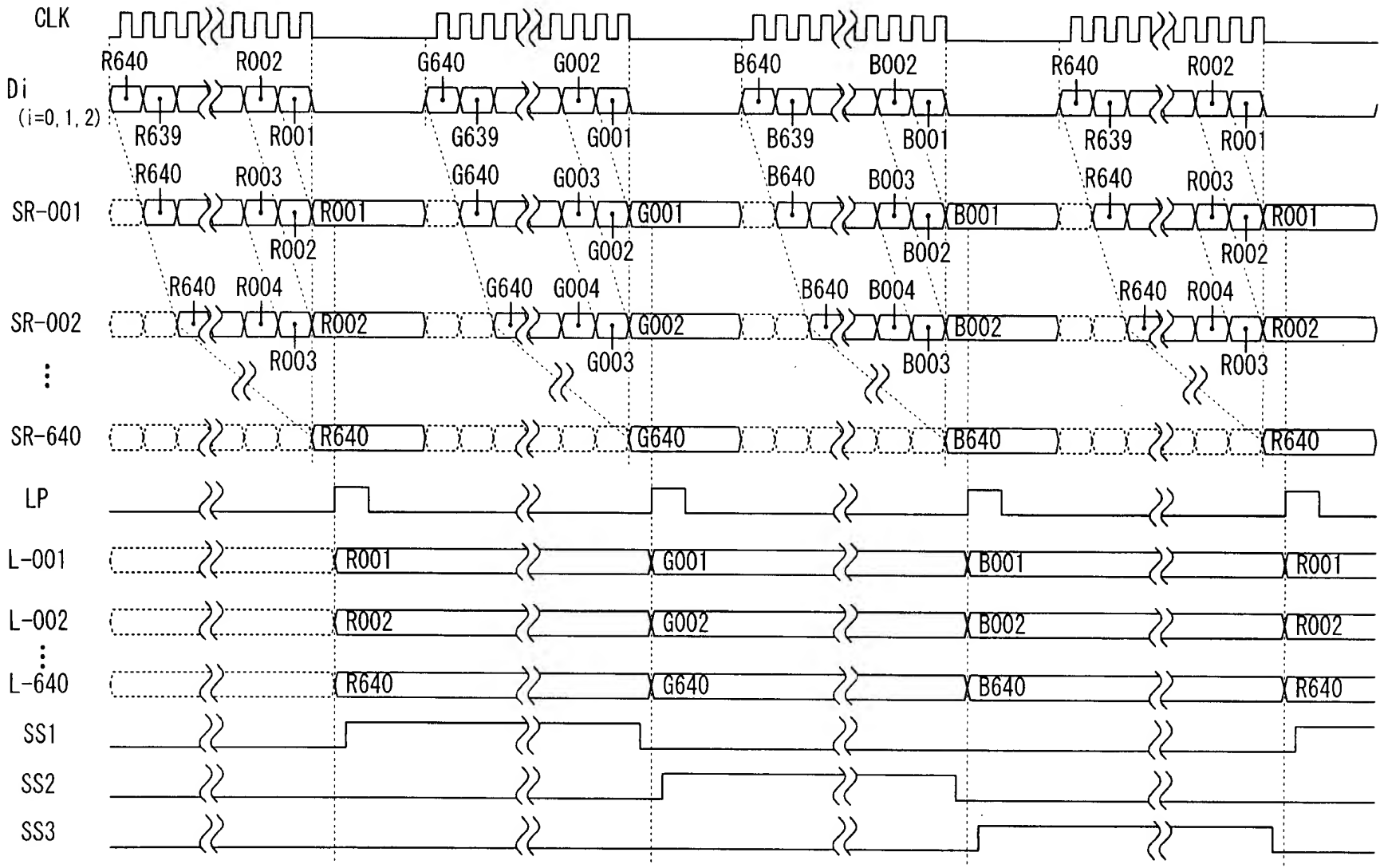

CLK
Di
(i=0, 1, 2)
R640
R002
G640
G002
B640
B002
R640
R002
R639
R001
G639
G001
B639
B001
R639
R001
SR-001
R640
R003
G640
G003
B640
B003
R640
R003
R001
G001
B001
R001
R002
G002
B002
R002
SR-002
R640
R004
G640
G004
B640
B004
R640
R004
R002
G002
B002
R002
R003
G003
B003
R003
SR-640
R640
G640
B640
R640
LP
L-001
R001
G001
B001
R001
L-002
R002
G002
B002
R002
L-640
R640
G640
B640
R640
SS1
SS2
SS3

FIG. 11

FIG. 12A

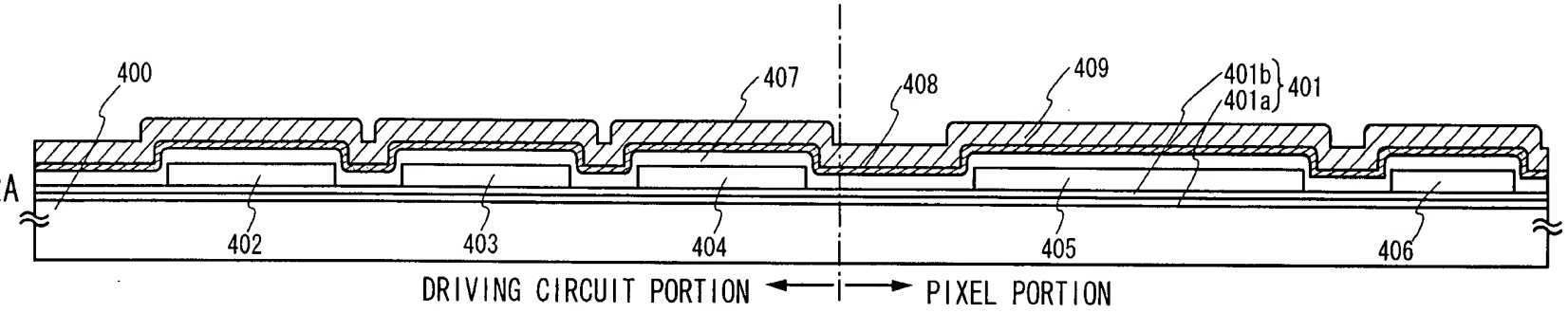


FIG. 12B

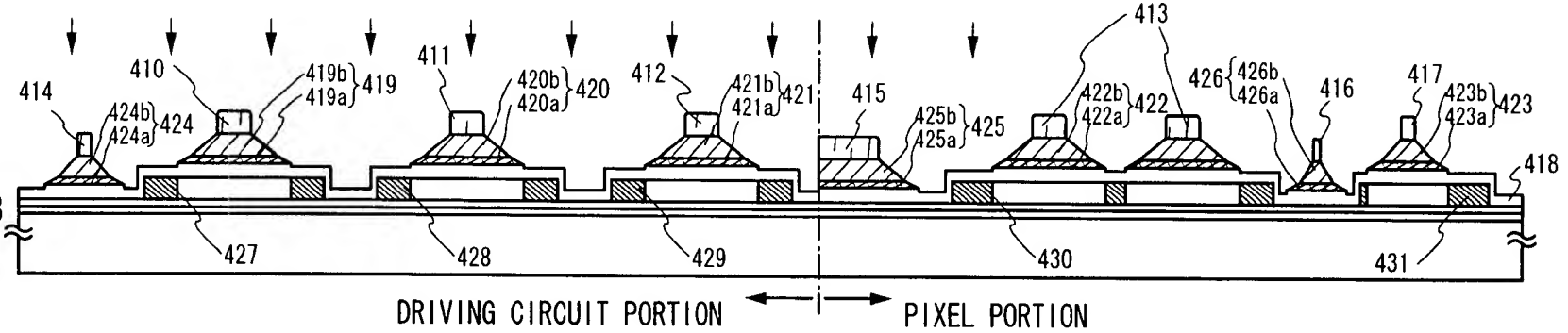


FIG. 12C

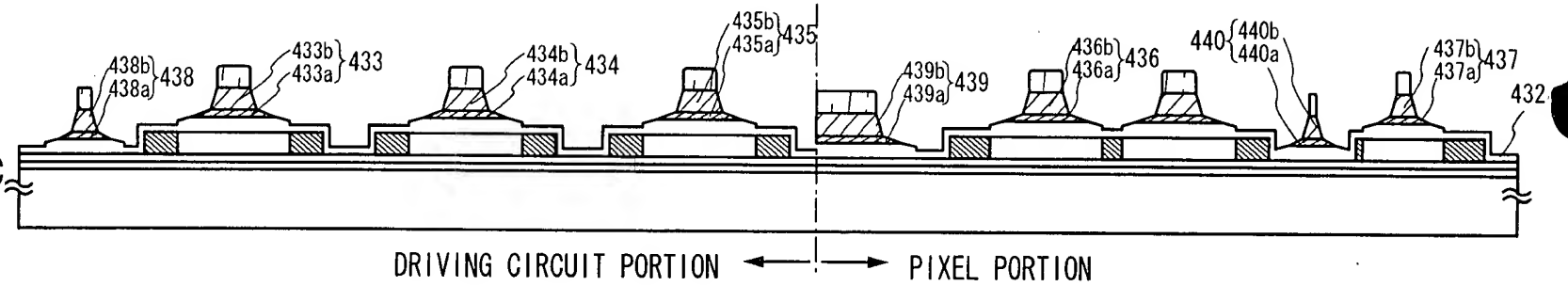


FIG. 13A

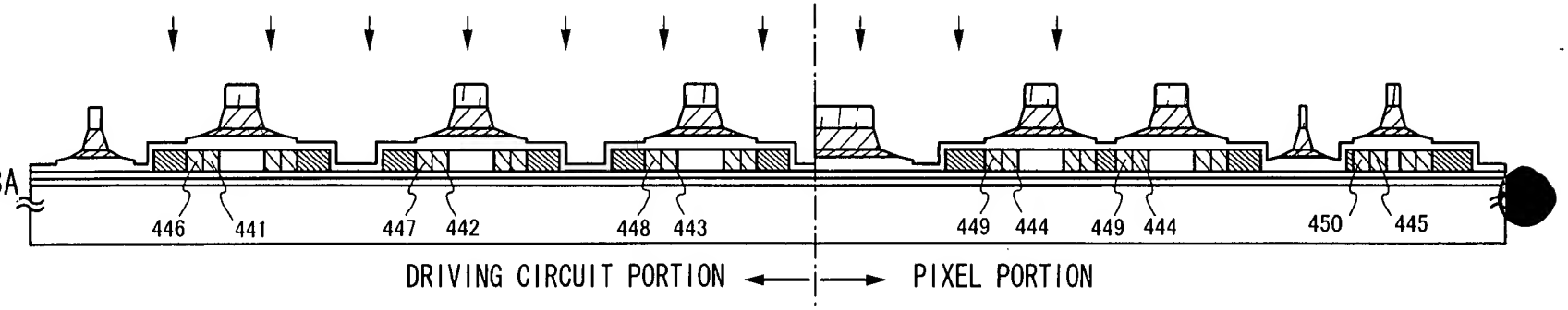


FIG. 13B

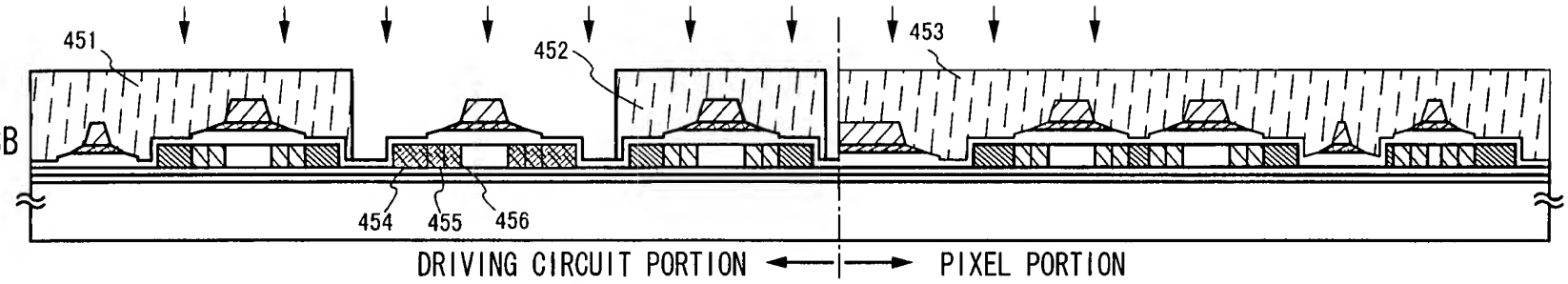
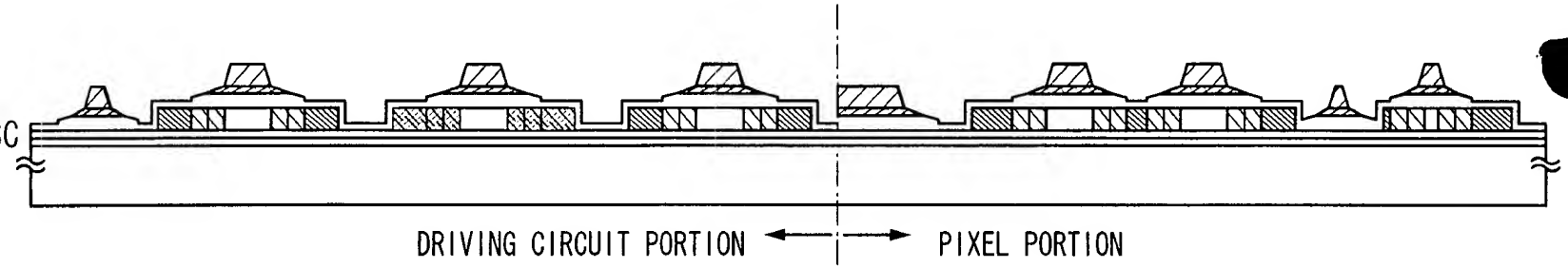


FIG. 13C



EP 0 820 084 A2

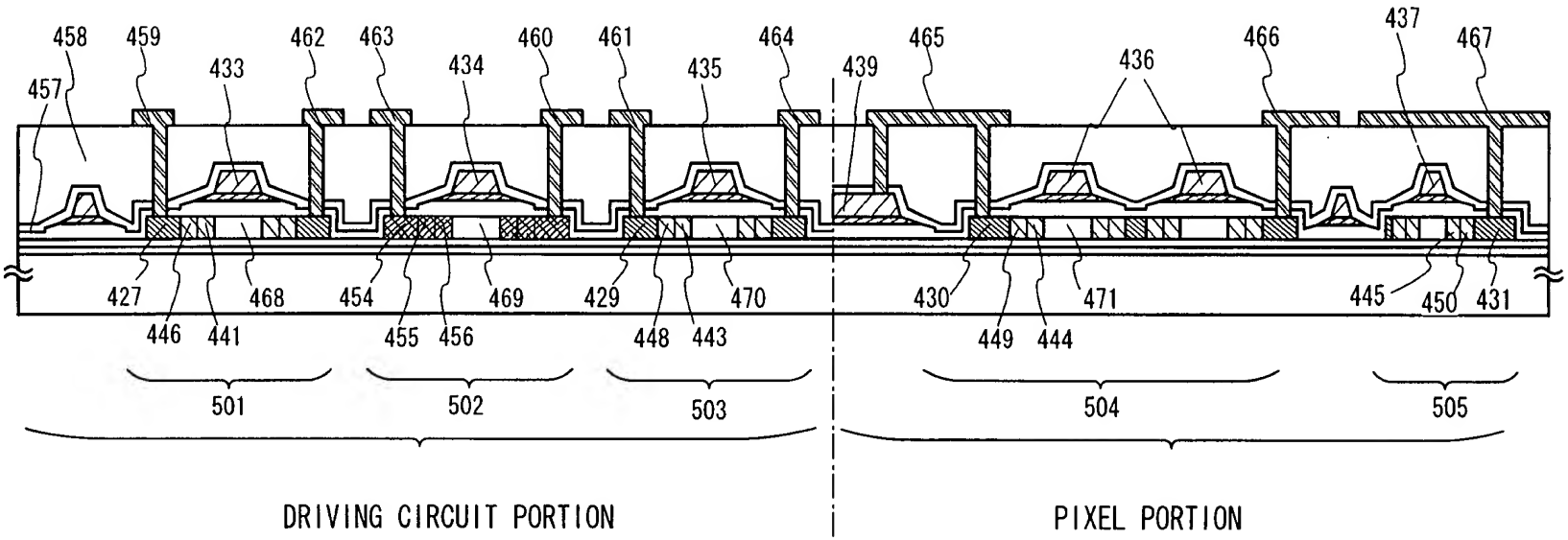


FIG. 14

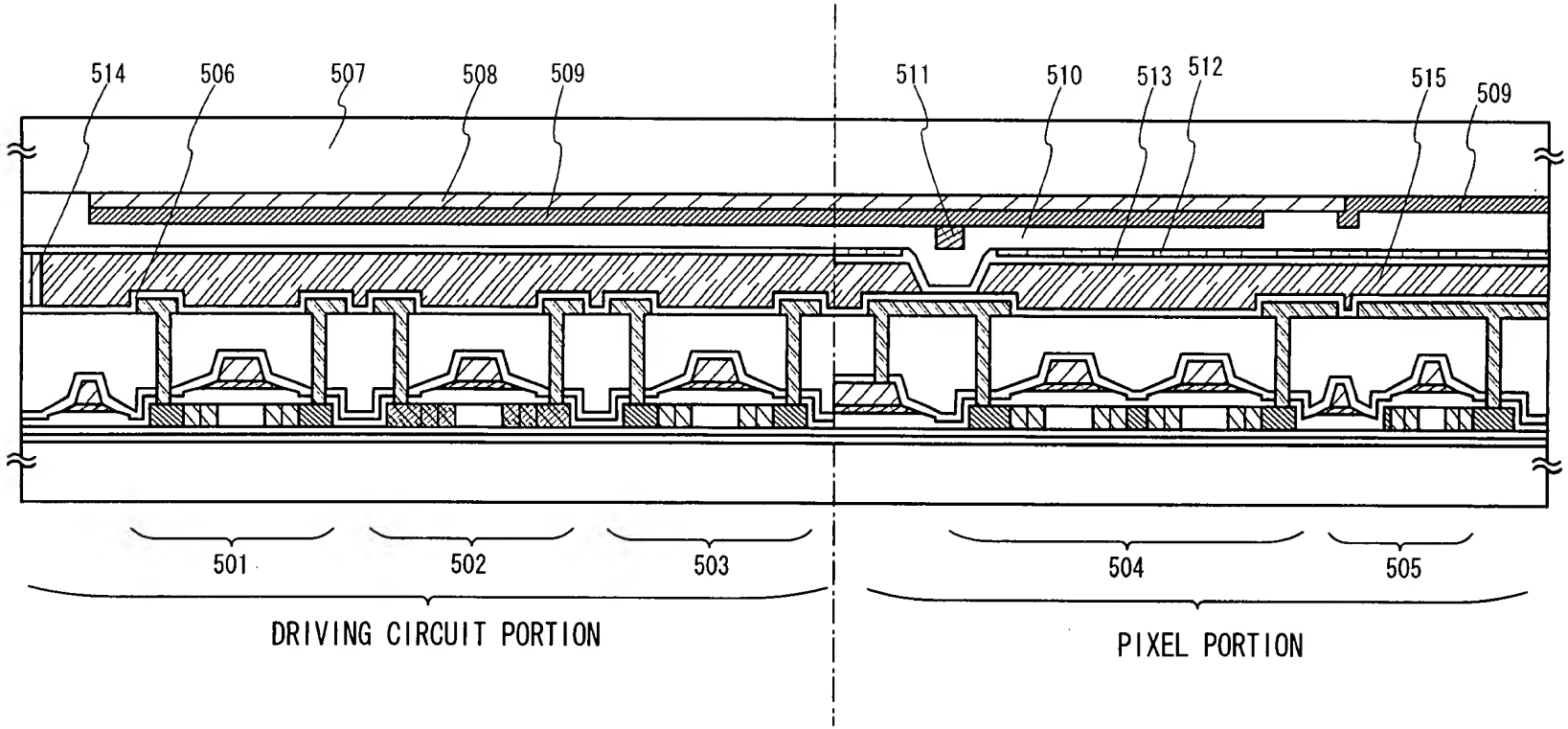

514
506
507
508
509
511
510
513
512
515
509
501
502
503
504
505
DRIVING CIRCUIT PORTION
PIXEL PORTION

FIG. 15

EP 3 503 203 A2

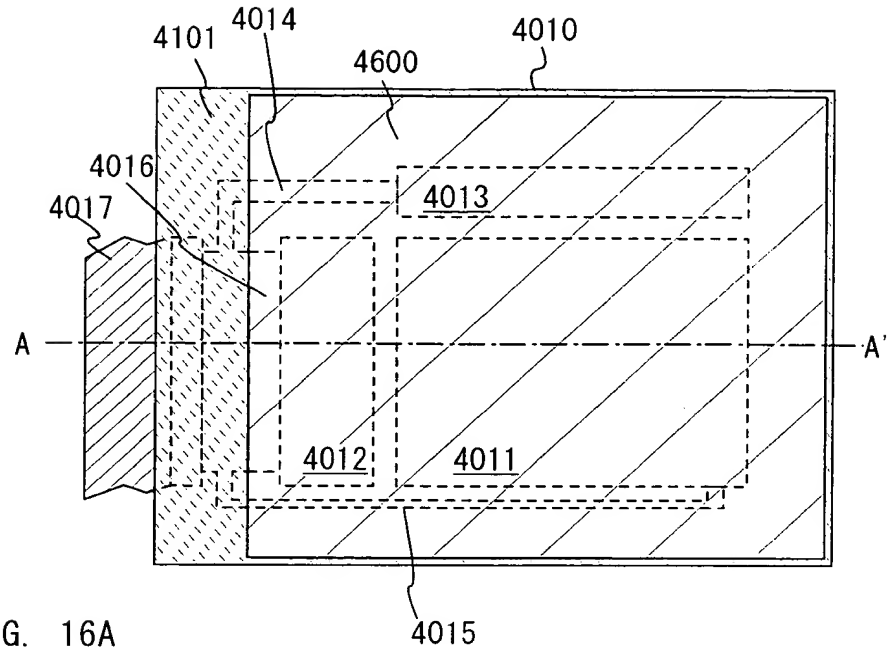


FIG. 16A

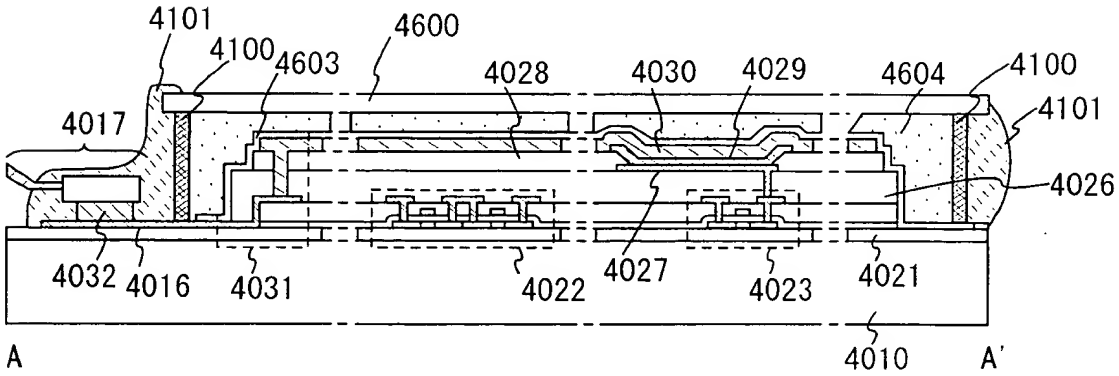


FIG. 16B

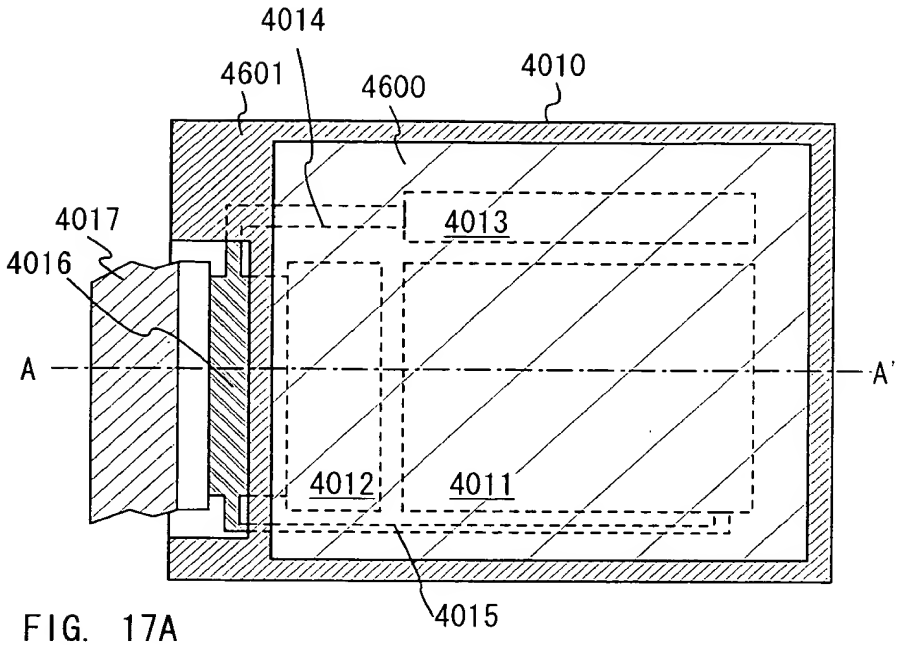


FIG. 17A

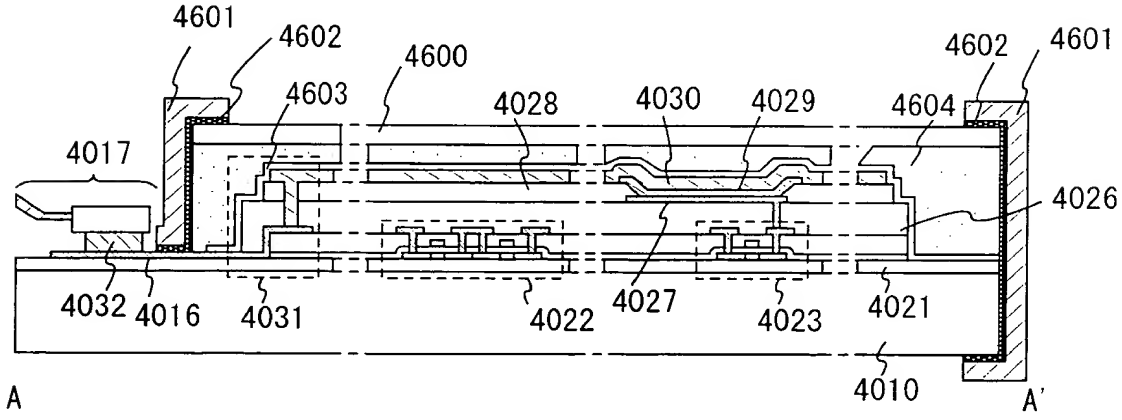


FIG. 17B

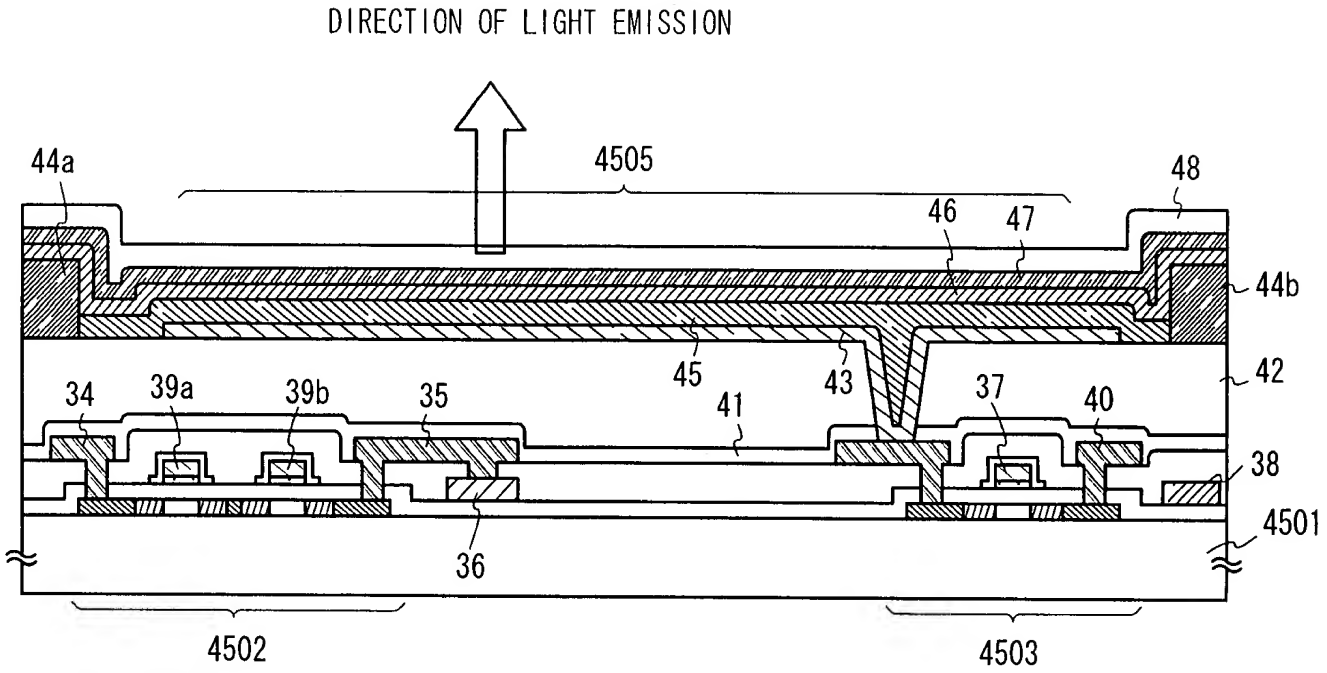

DIRECTION OF LIGHT EMISSION
44a
4505
48
46
47
44b
45
43
42
34
39a
39b
35
41
37
40
38
4501
36
4502
4503

FIG. 18

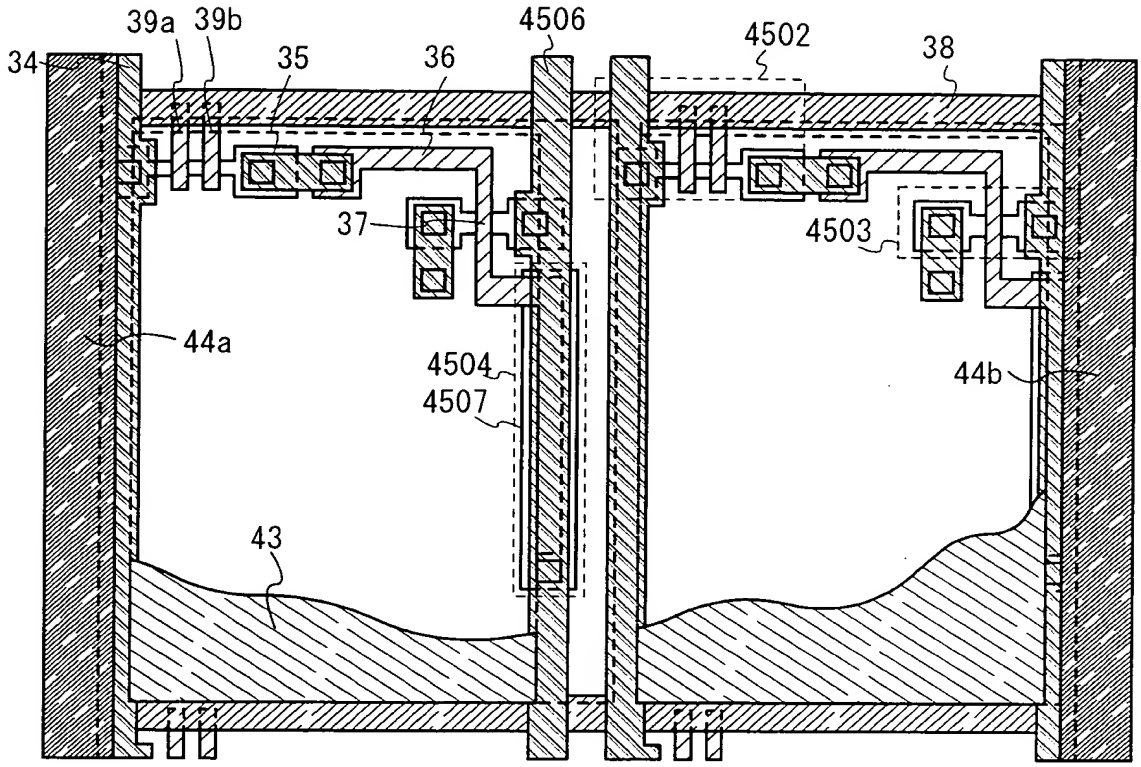


FIG. 19A

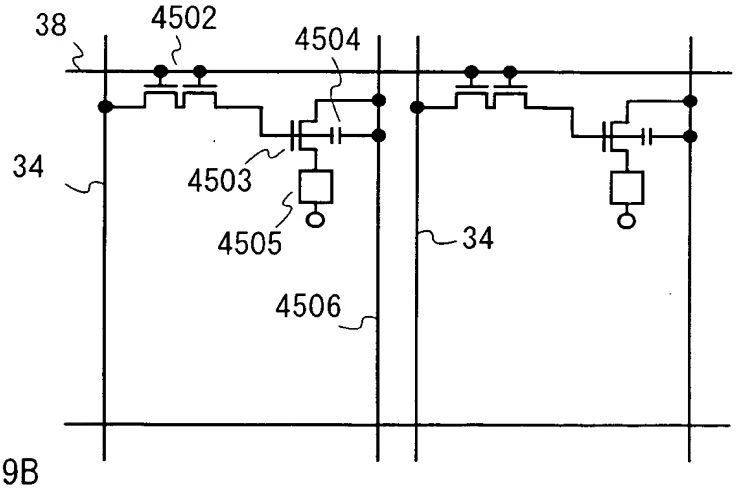


FIG. 19B

FOREIGN PATENT

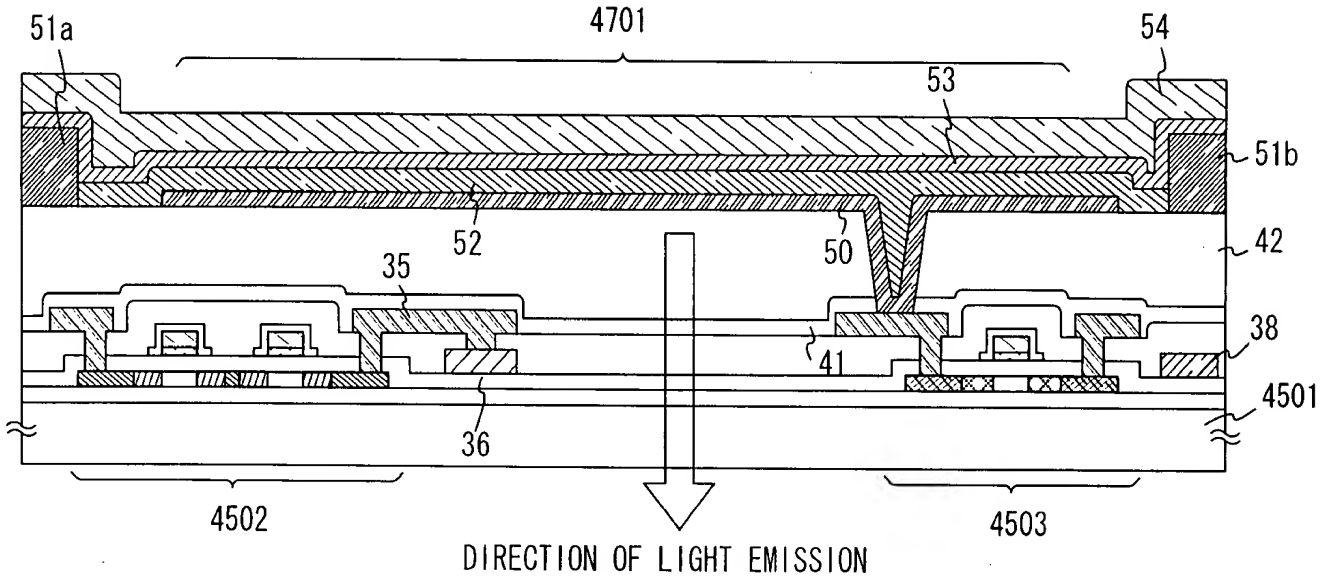


FIG. 20

FIG. 21A

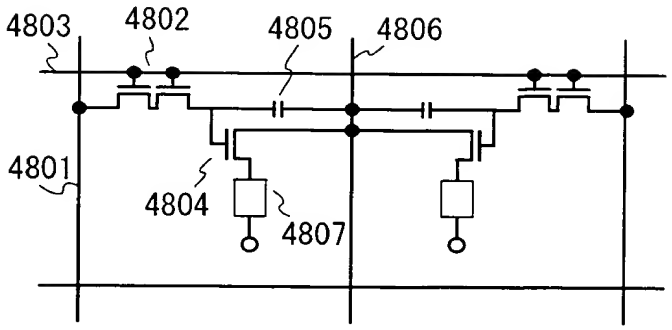


FIG. 21B

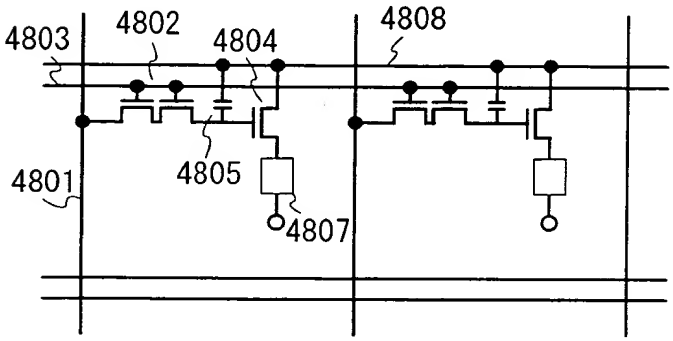
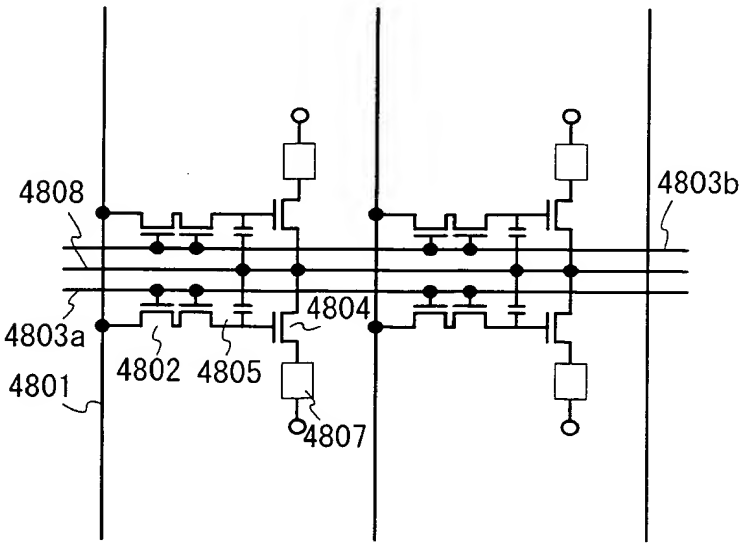


FIG. 21C



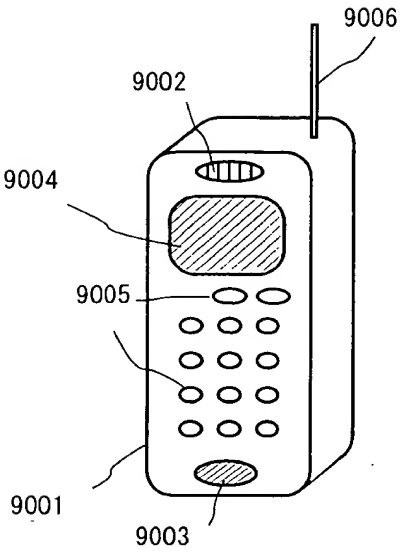


FIG. 22A

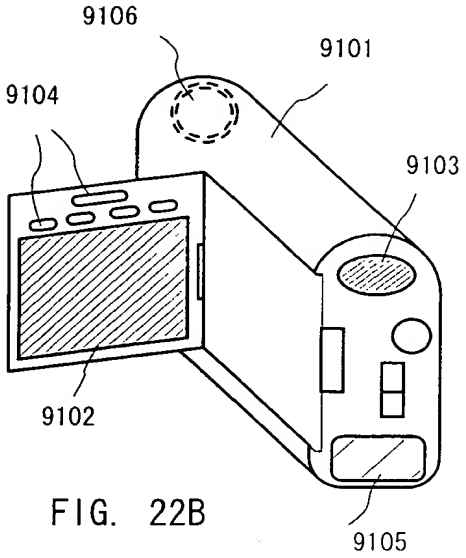


FIG. 22B

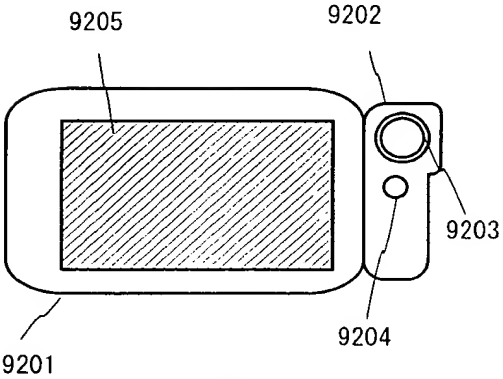


FIG. 22C

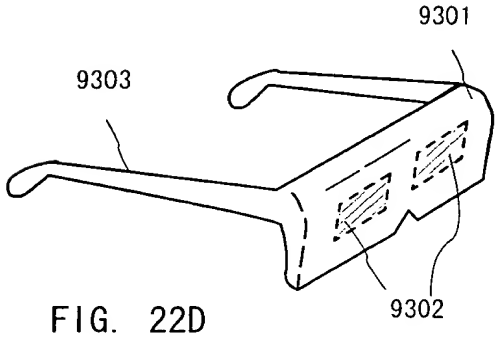


FIG. 22D

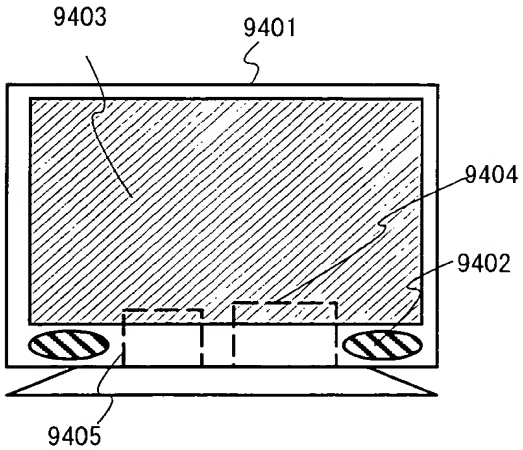


FIG. 22E

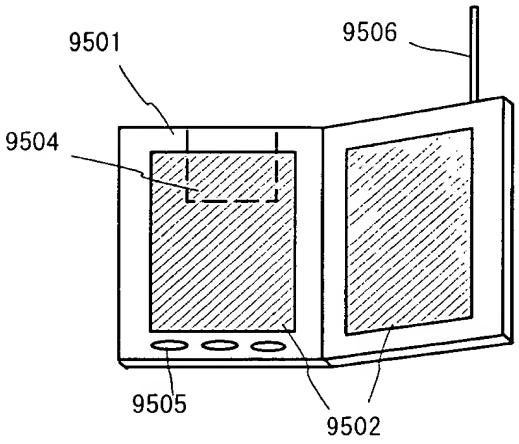


FIG. 22F

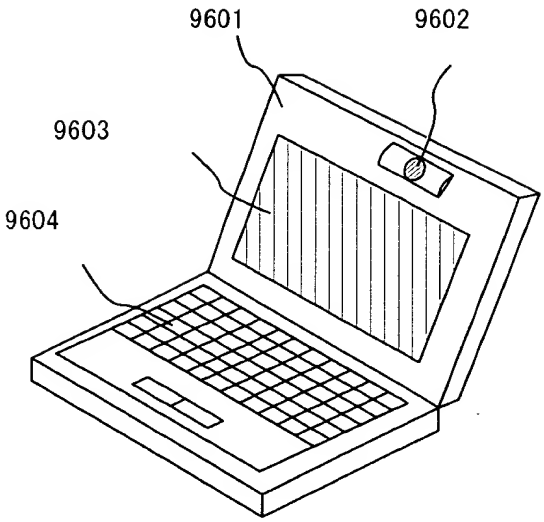


FIG. 23A

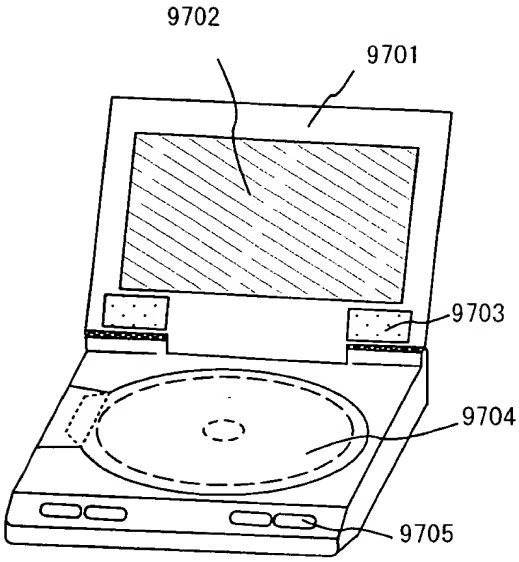


FIG. 23B

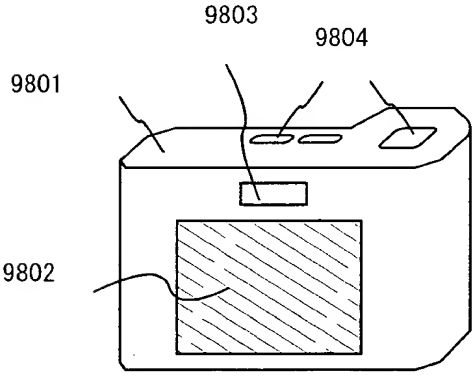


FIG. 23C

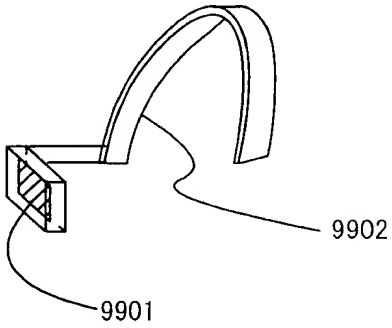


FIG. 23D

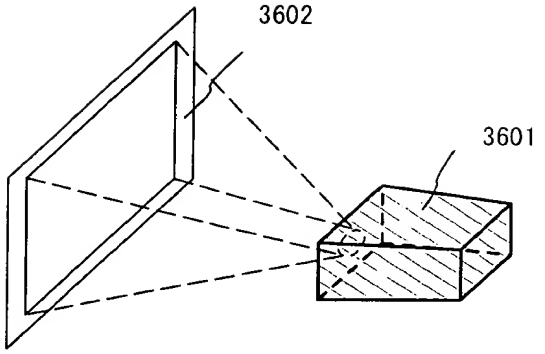


FIG. 24A

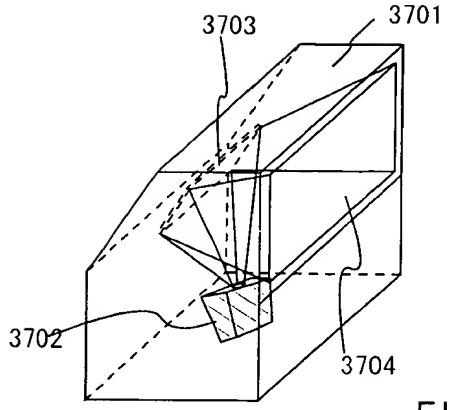


FIG. 24B

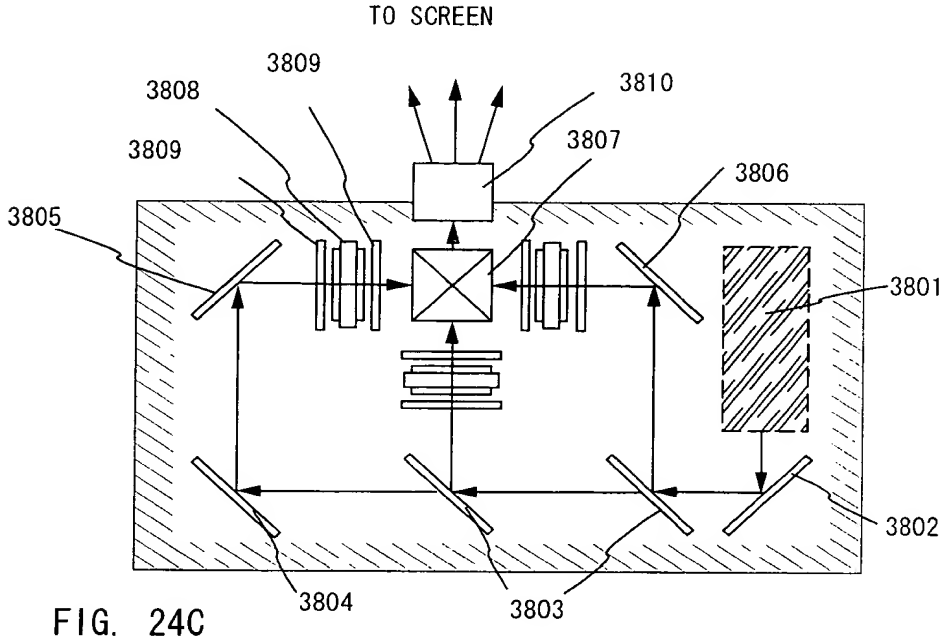


FIG. 24C

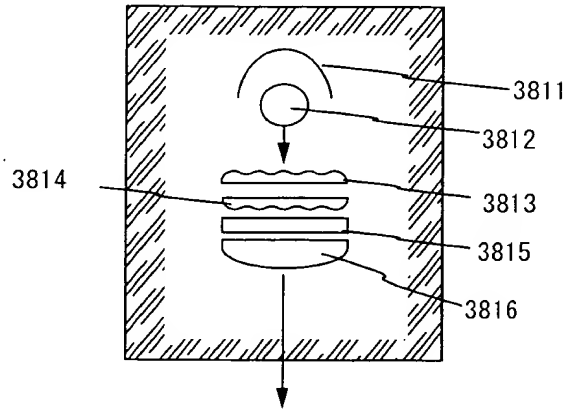


FIG. 24D

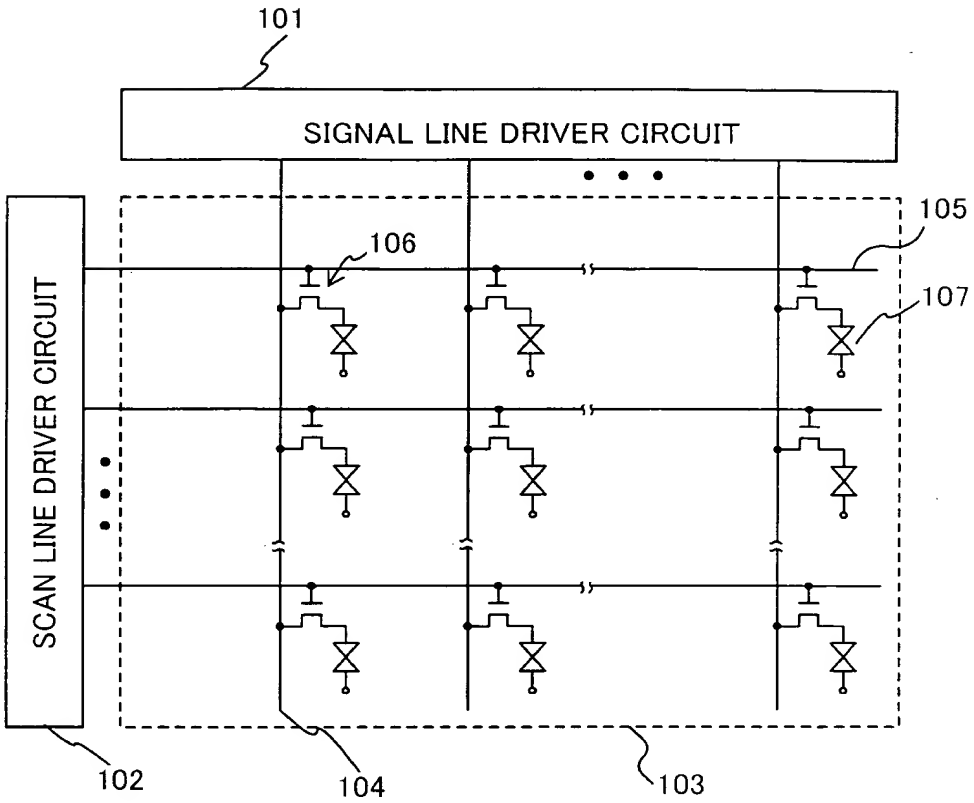

101
SIGNAL LINE DRIVER CIRCUIT
SCAN LINE DRIVER CIRCUIT
105
106
107
102
104
103

FIG. 25

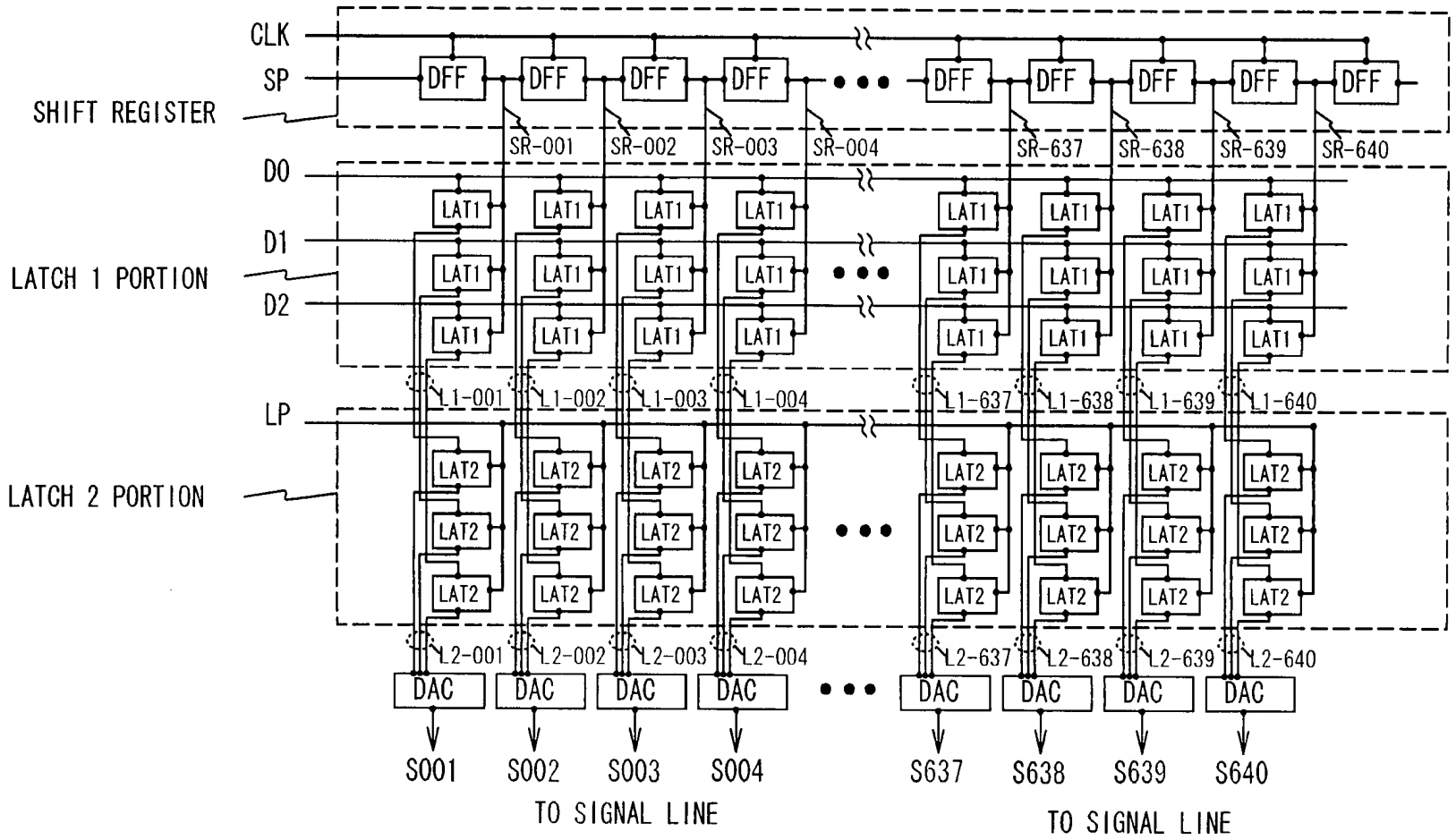

CLK
SP
SHIFT REGISTER
DFF
SR-001
SR-002
SR-003
SR-004
SR-637
SR-638
SR-639
SR-640
D0
D1
D2
LATCH 1 PORTION
LAT1
L1-001
L1-002
L1-003
L1-004
L1-637
L1-638
L1-639
L1-640
LP
LATCH 2 PORTION
LAT2
L2-001
L2-002
L2-003
L2-004
L2-637
L2-638
L2-639
L2-640
DAC
S001
S002
S003
S004
S637
S638
S639
S640
TO SIGNAL LINE
TO SIGNAL LINE

FIG. 26

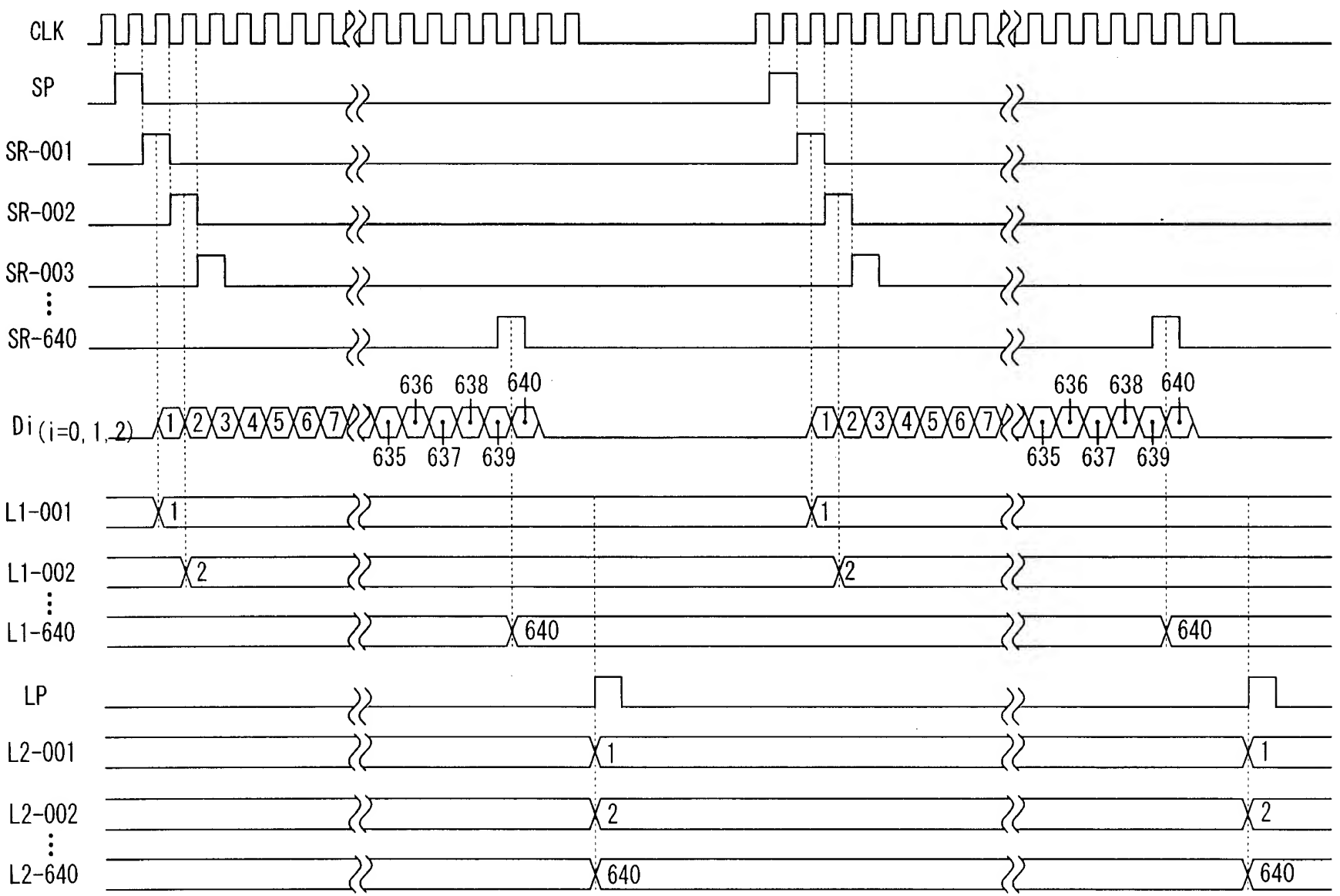

CLK
SP
SR-001
SR-002
SR-003
SR-640
Di (i=0, 1, 2)
636 638 640
635 637 639
L1-001
L1-002
L1-640
LP
L2-001
L2-002
L2-640

FIG. 27